REMARKS

Reconsideration and allowance are respectfully requested.

Before entry of this amendment, claims 1-20 were pending. In the Office Action, claims 1-3, 8-11, 14-20 were rejected, and claims 4-7 and 12-13 were allowed. In the present amendment, claims 16-17 are amended. After entry of the amendment, claims 1-20 are pending.

I. Claims 1-2 and 11

Claims 1-2 and 11 are rejected under 35 U.S.C. § 102(e) as being anticipated by Mergard et al. (USP 6,401,156) (Office Action, p. 3, lines 4-5). Applicant respectfully disagrees and traverses the § 102(e) rejection.

A. Independent claim 1

Mergard does not form the basis for a valid rejection under § 102(e) because Mergard does not disclose all of the limitations of claim 1. Claim 1 recites five elements of a microcontroller integrated circuit: "a terminal", "a crystal oscillator circuit", "a real time clock", "a processor" and "a clock multiplier circuit". Mergard discloses none of the terminal, the crystal oscillator circuit or the clock multiplier circuit.

The Examiner does not point to any structures in Mergard that disclose the terminal or the clock multiplier circuit. The Examiner points, however, to figures 2 and 10 of Mergard and states that the crystal oscillator circuit is disclosed as clock 124. (Office Action, page 3, lines 6-7)

Mergard does not disclose that the elements depicted in figures 2 and 10 are the elements of a microcontroller integrated circuit. To the contrary, figure 2 of Mergard is a diagram that illustrates some of the basic discrete hardware features of a personal computer, including DRAM, ROM, a keyboard subsystem, an ISA bus, clock 124 and microprocessor 100. Mergard does not disclose that these hardware features are on the same integrated circuit. Indeed, Mergard

states that processor 100 is a microprocessor based upon the Intel 8088. Thus, processor 100 is an integrated circuit separate and apart from clock 124. The real time clock 116 and clock 124 of Mergard are not disclosed as being on the same integrated circuit as processor 100.

The Examiner does not state that Mergard discloses a clock multiplier circuit. Instead, the Examiner states that "Mergard et al. discloses in Figs. 2&10 a microcontroller integrated circuit, comprising . . . an inherent clock multiplier circuit." (Office Action, p. 3, lines 6-12) (emphasis added). Applicant respectfully disagrees. Mergard does not disclose a microcontroller integrated circuit comprising an inherent clock multiplier circuit. Nothing in Mergard discloses or even suggests that the integrated circuit of processor 100 includes a clock multiplier circuit.

It is figure 1 of Mergard that shows a microcontroller, as opposed to figure 2, which shows the components of a personal computer. Mergard suggests that the microcontroller M of figure one is "a single monolithic integrated circuit" (Mergard, col. 7, line 59). Nevertheless, figure 1 of Mergard does not disclose a crystal oscillator circuit coupled to a terminal of the microcontroller integrated circuit. Moreover, figure 1 of Mergard does not disclose a clock multiplier circuit that generates a second clock signal that is supplied to the processor of the microcontroller integrated circuit.

Finally, the Examiner has not presented a *prima facie* argument of anticipation. Anticipation under § 102 requires the presence in a single prior art reference that discloses all of the elements of a claimed invention arranged as in the claim. Sandt Tech., Ltd. v. Resco Metal & Plastics Corp., 264 F.3d 1344, 1350 (Fed.Cir. 2001). "To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991)"

Metabolite Labs., Inc. v. Lab. Corp. of Am. Holdings, 370 F.3d 1354, 1367 (Fed. Cir. 2004) (emphasis added).

Under the principles of inherency, only if the structure disclosed in Mergard necessarily includes a microcontroller integrated circuit that comprises at least both a processor and a clock multiplier circuit is claim 1 anticipated. Mergard does not disclose or suggest that it is necessary for either the integrated circuit of microprocessor 100 of figure 2 or the integrated circuit of microcontroller M of figure 1 to include a clock multiplier circuit. Therefore, the Examiner has not established a *prima facie* case of anticipation under § 102(e) based on inherency.

Thus, Mergard does not form the basis for a valid rejection under § 102(e) because Mergard does not disclose all of the limitations of claim 1. Reconsideration of the § 102(e) rejection and allowance of claim 1 are requested.

B. Dependent claims 2 and 11

Claim 11 recites that the second clock signal generated by the crystal oscillator circuit can be output onto a second terminal of the microcontroller integrated circuit. Mergard does not disclose a crystal oscillator circuit on a microcontroller integrated circuit that outputs a clock signal onto a terminal of the microcontroller integrated circuit. Because Mergard does not disclose all of the limitations of claim 11, Mergard does not form the basis for a valid rejection under § 102(e).

Claims 2 and 11 depend from claim 1. In addition to the reasons explained above, dependent claims 2 and 11 are allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 102(e) rejection and allowance of claims 2 and 11 are requested.

III. Rejection of claims 3 and 8-10

Claims 3 and 8-10 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard in view of Ferraiolo et al. (US Patent No. 5,757,238) (Office Action, p. 4, lines 1-2). To established a *prima facie* case of obviousness, the Examiner must demonstrate three criteria. The MPEP § 2142 states:

> "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the reference (or references when combined) must teach or suggest all the claimed limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure . . .. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.' Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985)." MPEP § 2142 (emphasis added).

A. Dependent claim 3

Claim 3 recites "wherein the clock multiplier circuit includes a frequency locked loop, the frequency locked loop including a digital filter." The Examiner states,

> ". . . Mergard et al. does not discloses details of the clock multiplier circuit . . .. Ferraiolo et al. teaches in Fig. 2 a clock multiplier circuit . . .. Therefore, it would have been obvious to one of ordinary skill in the art to implement the clock multiplier circuit taught by Ferraiolo et al. with the prior art (Fig. 2 of Mergard et al.) in order to quickly achieve phase lock at the different operating frequency for the circuit" (Office Action, p. 4. lines 4-12).

The combination of Mergard and Ferraiolo does not form the basis for a valid rejection under § 103(a) for two reasons. First, the references when combined do not teach or suggest all of the claim elements. Second, there is no suggestion or motivation in either Ferraiolo or Mergard to combine the teaching of one with the teachings of the other.

First, neither Mergard nor Ferraiolo teaches or suggests a microcontroller integrated circuit comprising a processor, a crystal oscillator circuit and a clock multiplier circuit, wherein the clock multiplier circuit includes a frequency locked loop. Mergard does not disclose a clock multiplier circuit. Moreover, Ferraiolo does not disclose a microcontroller integrated circuit with a clock multiplier circuit. Thus, Ferraiolo does not disclose using the phase-locked loop (200) as a clock multiplier circuit in an integrated circuit that also comprises a crystal oscillator circuit and a processor. Finally, neither Mergard nor Ferraiolo teaches or suggests a frequency locked loop. Instead, Ferraiolo discloses a phase-locked loop (200).

Second, the Examiner points to no suggestion or motivation in Mergard to combine the teachings of Mergard with the teachings of Ferraiolo. There is no suggestion in either Mergard or Ferraiolo to use the phase-locked loop (200) of Ferraiolo as a clock multiplier circuit on a microcontroller integrated circuit. The Examiner states that "it would have been obvious to one of ordinary skill in the art to implement the clock multiplier circuit taught by Ferraiolo et al. with the prior art (Fig. 2 of Mergard et al.) in order to quickly achieve phase lock at the different operating frequency for the circuit" (Office Action, p. 4, lines 9-12). But there is no suggestion in either Mergard or Ferraiolo to integrate a clock multiplier circuit into a microcontroller integrated circuit. It would not have been obvious to incorporate the phase-locked loop of Ferraiolo into an "inherent" (but undisclosed) clock multiplier circuit of Mergard to obtain a microcontroller integrated circuit comprising a processor, a crystal oscillator circuit and a clock multiplier circuit with a frequency locked loop.

Because the combination of Mergard and Ferraiolo does not disclose all of the elements of claim 3, and furthermore because there is no suggestion or motivation to combine Mergard and Ferraiolo, Mergard and Ferraiolo do not form the basis for a valid rejection under § 103(a). In addition, claim 3 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 3 is requested.

B. Dependent claims 8-10

Claims 8-10 depend from claim 1 and are allowable for at least the same reasons for which claim 1 is allowable. The rejection of claims 8-10 should therefore be withdrawn. Reconsideration and allowance is requested.

IV. Rejection of claim 14

Claim 14 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard (Office Action, p. 4, line 14). The Examiner states that "Mergard et al. meets all of the claimed limitations except for the intended use [of] the microcontroller in a battery-powered device" (Office Action, page 4, lines 15-16). Claim 14 does not recite that the microcontroller is intended to be used in a battery-powered device. Instead, claim 14 recites, "the microcontroller is part of a battery-powered device."

Mergard does not form the basis for a valid rejection under § 103(a) because Mergard does not disclose all of the limitations of claim 14. Mergard does not discloses a microcontroller integrated circuit comprising a processor and a clock multiplier circuit. Thus, Mergard also does not disclose such a microcontroller that is part of a battery-powered device. Moreover, there is no expectation of success that even the monolithic integrated circuit shown in figure 1 of Mergard could function in a battery-powered device.

In addition, Mergard does not disclose a clock multiplier circuit on a microcontroller integrated circuit that receives a first clock signal with a frequency less than 5 MHz and generates therefrom a second clock signal with a frequency greater than 100 MHz. The Examiner suggests that multiplying a frequency of less than 5 MHz to a frequency greater than 100 MHz recites a certain range within a range taught by Mergard. (See Office Action, page 4, line 21 - page 5, line 5) Mergard, however, does not teach a clock multiplier circuit on a microcontroller integrated circuit that multiplies a frequency to any degree. Mergard does not disclose multiplying (as opposed to dividing) a clock signal on chip.

Mergard does not form the basis for a valid rejection of claim 14 under § 103(a) because Mergard does not teach all of the claim limitations. In addition, claim 14 depends from claim 1 and is allowable for at least the same reasons for which claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 14 is requested.

V. Rejection of claim 15

Claim 15 is rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard in view of Gulliver et al. (US Patent No. 6,150,889) (Office Action, p. 5, lines 6-7). Claim 15 recites, "a third clock signal on the second terminal can be supplied to the clock input lead of the clock multiplier circuit." The combination of Mergard and Gulliver does not form the basis for a valid rejection under § 103(a) because the references when combined do not teach or suggest all of the claim elements. Neither Mergard nor Gulliver teaches selectively supplying clock signals that are present on terminals of a microcontroller integrated circuit to a clock multiplier circuit on the integrated circuit, such that the signal generated by the clock multiplier circuit is supplied to a processor on the integrated circuit.

Claim 15 depends from claim 1. In addition to the reason explained above, dependent claim 15 is allowable for at least the same reasons for which

claim 1 is allowable. Reconsideration of the § 103(a) rejection and allowance of claim 15 is requested.

VI. Claims 16-20

Claims 16-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Mergard in view of Adams (US Patent No. 5,638,010) (Office Action, p. 5, lines 17-18). Claim 16 as amended recites, "An integrated circuit, comprising: a processor . . . and a frequency locked loop coupled to a low frequency external crystal exhibiting a first frequency, wherein the frequency locked loop receives a first clock signal . . . and generates therefrom a second clock signal, . . . wherein the second clock signal is supplied to the clock input lead of the processor."

The combination of Mergard and Adams does not form the basis for a valid rejection under § 103(a) because the references when combined do not teach or suggest all of the claim elements. Neither Mergard nor Adams teaches a processor and a frequency locked loop on an integrated circuit, wherein the frequency locked loop receives a signal from a low frequency external crystal and supplies a signal to the clock input lead of the processor. Moreover, neither Mergard nor Adams teaches a frequency locked loop. The Examiner states that "Adams teaches in Figs. 3-6 a circuit having a frequency locked loop . . ." (Office Action, page 6, line 11). Figure 3 of Adams, however, shows a phase-locked loop, as evident from phase detector 80.

In addition, there is no suggestion in either Mergard or Adams to include the phase-locked loop of Adams in the microcontroller integrated circuit of figure 1 of Mergard in order to use an slow external crystal to clock a processor.

Claim 17 depends from claim 16 and is allowable for at least the same reasons for which claim 16 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 16 and 17 is requested.

Claim 18 recites, "A device, comprising: a processor on a microcontroller integrated circuit; a 32,768-hertz crystal external to the microcontroller integrated circuit; and means for using the 32-768-hertz crystal to clock the processor at a

frequency higher than 100 megahertz, wherein the means generates a ramp signal."

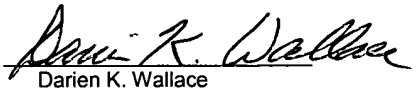
Neither Mergard nor Adams teaches a processor on an integrated circuit that is clocked by a 32,768-hertz crystal external to the microcontroller integrated circuit. Neither Mergard nor Adams teaches clocking a processor by multiplying the signal from an external 32,768-hertz crystal.

Claims 19 and 20 depend from claim 18 and are allowable for at least the same reasons for which claim 18 is allowable. Reconsideration of the § 103(a) rejection and allowance of claims 18-20 is requested.

VII. Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully submits that the entire application (claims 1-20 are pending) is in condition for allowance. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. The undersigned can be contacted at (925) 621-2121 to discuss any aspect of this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

By 
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